

## REMARKS

The Examiner's Office Action of June 7, 2004 has been received and its contents reviewed. Applicant would like to thank the Examiner for the consideration given to the above-identified application.

By the above actions, claims 10, 27, 45 and 62 have been amended, claims 11-18, 28-35, 46-53 and 63-70 have been cancelled, and new claims 105-123 have been added. Accordingly, claims 1-10, 19-27, 36-45, 54-62, and 71-123 are pending for consideration, of which claims 1, 19, 36, 54, 71, 80, 88, 97, 105 and 115 are independent. In view of these actions and the following remarks, reconsideration of this application is now requested.

Referring now to the detailed Office Action, the drawings are objected to under 37 C.F.R. 1.83(a). Specifically, the Examiner objects to the drawings because the limitation "a multiple of m shift registers" of claims 1, 19, 36, 54, 71, 80, 88 and 97 must be shown in the drawings or the feature(s) canceled from the claims. In response, Applicant has added new Figure 28, as attached herewith, that shows "a multiple of m shift registers". Figure 28 is in accordance with the description found on page 12, line 24 through page 13, line 5 and FIG. 1. Figure 28 shows the following features: 3-bit digital picture signal (D0, D1, D2) is divided into two signals (D0(A), D0(B), D1(A), D1(B), D2(A), D2(B)); the number of shift registers is  $3(\text{bits}) \times 2(\text{the division number}) = 6$ ; and the number of DFFs contained in the respective shift registers is decreased by half correspondingly to the division. Figure 28 does not include any new matter because Figure 28 is fully supported by page 12, line 24 through page 13, line 5 and FIG. 1 of the specification.

In spite of the submission of new Fig. 28, Applicant respectfully traverses the objection to the drawings because such a level of detail rendering of the number of shift registers being multiple of m, as required by the Examiner, is deemed unnecessary. Further, as "the number of shift registers being multiple of m" can be easily understood based on Fig. 1 and its description in the present application, Applicant did not show such a level of detail in Fig. 1. In view of the above, the objection to the drawings is respectfully requested to be reconsidered and withdrawn.

Claims 1-8, 19-25, 71-79, 80-87 stand rejected under 35 U.S.C. §103(a) as unpatentable over Matsushima (U.S. Patent No. 6,256,079 B1 – hereafter Matsushima) in view of Lewis (U.S. Patent No. 5,589,847 – hereafter Lewis) and Lüder et al. (U.S. Patent

No. 5,642,117 – hereafter Lüder). Further, claims 36-43, 54-60, 88-96 and 97-104 stand rejected under 35 U.S.C. §103(a) as unpatentable over Matsushima in view of Lewis, Lüder et al. and Kinoshita et al. (U.S. Patent No. 5,771,031 – hereafter Kinoshita).

Still further, claims 9, 26, 44 and 61 stand rejected under 35 U.S.C. §103(a) as unpatentable over Lewis, Matsushima, Kinoshita et al. and Lüder in view of Friend et al. (U.S. Patent No. 5,247,190 – hereafter Friend). Finally, claims 10-18, 27-35, 45-53 and 62-70 stand rejected under 35 U.S.C. §103(a) as unpatentable over Lewis, Matsushima and Kinoshita and Lüder in view of Matsueda et al. (U.S. Patent No. 6,384,806 B1 – hereafter Matsueda). These rejections are respectfully traversed at least for the reasons provided below.

With respect to the §103(a) rejection of claims 11-18, 28-35, 46-53 and 63-70 over Lewis, Matsushima and Kinoshita and Lüder in view of Matsueda, the cancellation of the above claims has rendered the rejection moot.

With respect to the rejections of the independent claims, the Examiner alleges that Lewis, which is a secondary reference cited in each of the §103(a) rejections, teaches shift registers to which m-bit digital picture signals are inputted, m x k/n storage circuits for converting output signals of the storage circuits into analog signals, and k/n signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines. However, Applicant respectfully asserts that Lewis, as well as the other cited prior art references, fails to teach, disclose or suggest the feature recited in independent claims 1, 19, 36, 54, 71, 80, 88, 97 directed to “shift registers to which m-bit (m is a natural number) digital picture signals are inputted.”

Moreover, Lewis, as well as the other cited prior art references, also fail to teach, disclose or suggest “the number of the shift registers being a multiple of m” as recited in Applicant’s independent claims. Therefore, Lewis cannot cure the deficiencies of Matsushima and the other applied prior art references, and the combination of the Lewis reference with the others is insupportable.

Notwithstanding the arguments set forth above, it is well settled that when combining the references in order to support a *prima facie* case of obviousness, the references must be considered in their entirety. It is further settled that the mere fact that the prior art may be modified to reflect features of the claimed invention does not make the modification and

hence the claimed invention obvious unless the desirability of such modification is suggested by the prior art itself (MPEP §2141). Moreover, the claimed invention cannot be used as an instruction manual or “template” to piece together the teachings of the prior art so that the claimed invention is rendered obvious, *In Re Fritsch*, 23 USPQ2d 1780 (Fed. Cir. 1992).

Further, the requirements for establishing a *prima facie* case of obviousness, as detailed in MPEP § 2143 - 2143.03 (pages 2100-122 - 2100-136), are: first, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference(s) to combine the teachings; second, there must be a reasonable expectation of success; and, finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations.

Applicant respectfully submits that the Examiner has failed to show that the combination of Matsushima and Lewis would teach or suggest all of Applicant’s claimed limitations. Further, the Examiner has failed to provide support for motivation or suggestion in each of the cited prior art references as to how their respective teachings may be combined to successfully arrive at Applicant’s claimed invention.

For example, as acknowledged by the Examiner, Matsushima discloses the number of shift registers in an LCD display with not less than 800 signal lines by an element equipped with at least four series of shift registers, or preferably eight series of shift registers (col. 2, lines 29-35 of Matsushima). The Examiner further acknowledges on page 3 of the Office Action that Matsushima fails to disclose shift registers to which  $m$ -bit ( $m$  is a natural number) digital picture signals are inputted,  $m \times k/n$  ( $n$  is an integer of not less than 2) storage circuits for storing output signals of the shift registers, a plurality of D/A converter circuits for converting output signals of the storage circuit into analog signals, and  $k/n$  ( $n$  is an integer of not less than 2) signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines.

Applicant respectfully asserts that the mere disclosure of at least for series of shift register or preferably eight series of shift register in Matsushima does not in anyway disclose or suggest that the number of shift register is multiple of  $m$ . Therefore, clearly, there is no suggestion or motivation in Matsushima to include shift registers to which  $m$ -bit ( $m$  is a

natural number) digital picture signals are inputted, wherein the number of the shift registers is a multiple of  $m$ , as recited in Applicant's pending independent claims.

Applicant respectfully further asserts that, although Lewis disclose shift registers, Lewis clearly does not disclose or suggest the number of the shift registers being a multiple of  $m$  and shift registers to which  $m$ -bit ( $m$  is a natural number) digital picture signals are inputted.

Hence, as Matsushima fails to teach, disclose or suggest  $m$ -bit shift registers wherein the number of shift registers is a multiple of  $m$ , and as Lewis does not teach, disclose or suggest the number of the shift registers being a multiple of  $m$  and shift registers to which  $m$ -bit ( $m$  is a natural number) digital picture signals are inputted, the combination of Lewis with Matsushima cannot be made. Even if these references were combined, the feature of the number of shift registers being a multiple of  $m$  would still be deficient.

Applicant respectfully directs the Examiner's attention to, e.g., page 18, lines 13 through 21 where solutions and advantages provided by Applicant's claimed invention are disclosed. It is stated therein the following:

*...in the present invention, although the number of shift registers is increased, it is possible to drive the image display device by the shift registers each made of circuits, the number of which is  $1/4$  of the related art, the storage circuit, the number of which is  $1/8$  of the related art, and the D/A converter circuit, the number of which is  $1/4$  of the related art, and it becomes possible to greatly reduce the occupied area of the driver circuit and the number of elements. Besides, since the digital picture is directly inputted to the shift register, it becomes possible to shorten the signal transmission line for supplying the digital picture signal, to make connected gate capacitance dramatically small, and to decrease the resistance and load capacitance of the signal transmission line.*

Applicant respectfully asserts that the cited Matsushima, the primary reference, and Lewis, as well as the other secondary references, do not appear to recognize the problems that the present invention is solving and, hence, do not teach Applicant's invention or provide a motivation to combine their teaching to arrive at Applicant's claimed invention.

In order to keep the prosecution history compact, and as Applicant's arguments set forth above are deemed sufficient to overcome all of the §103(a) rejections, Applicant will

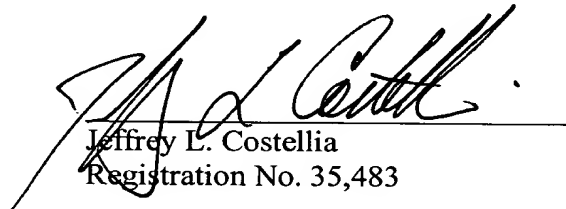
not respond to each and every §103(a) rejection. Applicant reserves the right to do so in the future, as necessary.

New claims 105-123 have been added to further complete the scope to which Applicant is entitled. New independent claims 105 and 115 are similar to claims 1 and 70, respectively, except for the limitation of the ramp type D/A converters.

In view of the amendments and arguments set forth above, Applicant respectfully requests reconsideration and withdrawal of all the pending rejections.

While the present application is now believed to be in condition for allowance, should the Examiner find some issue to remain unresolved, or should any new issues arise, which could be eliminated through discussions with Applicant's representative, then the Examiner is invited to contact the undersigned by telephone in order that the further prosecution of this application can thereby be expedited.

Respectfully submitted,



Jeffrey L. Costellia  
Registration No. 35,483

NIXON PEABODY LLP  
Suite 900, 401 9<sup>th</sup> Street, N.W.  
Washington, D.C. 20004-2128  
(202) 585-8000

JLC/LCD